24 Digital I/O with Digital Integration Features for Mini PCI Express and M.2

Hardware Manual

Models **mPCIe-DIO-24X, mPCIe-DIO-24A, M.2-DIO-24X, M.2-DIO-24A**



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MADE IN THE USA

Chapter 1: Quick Start

It is recommended that you install the software package before installing the M.2 or PCI Express Mini Card (mPCIe) in your computer. You can install the software[1] using either a stand-alone installer downloaded from the website or an optional Software Master CD.

Run the installer you downloaded (or autorun.exe on the Software Master CD) and follow the prompts to install the software for your device.

Please note: during the installation you may be prompted regarding the installation of non-WHQL-certified drivers; please carefully confirm the digitally signed source of the drivers and accept the installation.

Once the software has been installed, shut down your system and carefully install the M.2 or mPCIe card.

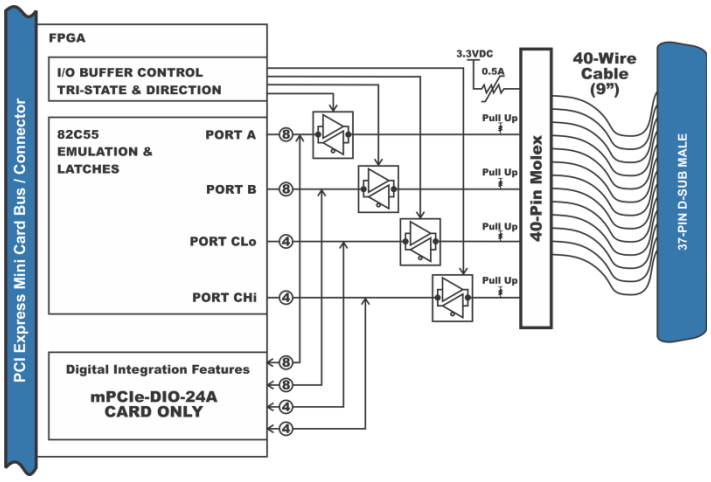
Re-start your system. Once the computer finishes booting, your new digital I/O should already be installed and ready for use; you can confirm this by launching Device Manager and looking under the "Data Acquisition" section. If, for any reason, the device displays a warning triangle, right-click and select "Update Driver".

[1] *In Linux or OSX please refer to the instructions in those directories.*

Chapter 2: Introduction

This manual applies to both the mPCIe-DIO-24X Digital I/O card, and the M.2-DIO-24X as they are register and functionally identical.

- mPCIe: type F1, with latching I/O connector
- M.2 Card: Type 2280-D3-B-M, breakaway to 2260-D3-B-M
- 24 high-current DIO lines (24mA source/sink)
- Change-of-State (CoS) detection IRQ generation
- 2x 8-bit and 2x 4-bit ports, independently selectable for inputs or outputs
- All signals brought out to an optional panel-mountable 37-pin male D-sub connector
- RoHS ships as standard



The advanced logic circuit supports a wide variety of features in addition to simple digital control or monitoring, and additional features can be created, just for you!

The mPCIe-DIO-24A introduces a wide array of advanced digital features, leveraging the power of the onboard FPGA. Available Digital Integration Features are as follows:

Input Features

- Optional De-bouncing
- Event counters with threshold IRQ
- Edge (rising/falling) and Pulse (high/low) Event counting
- Pulse (high/low) duration, Frequency, and duty-cycle (PWM) measurement, simultaneously

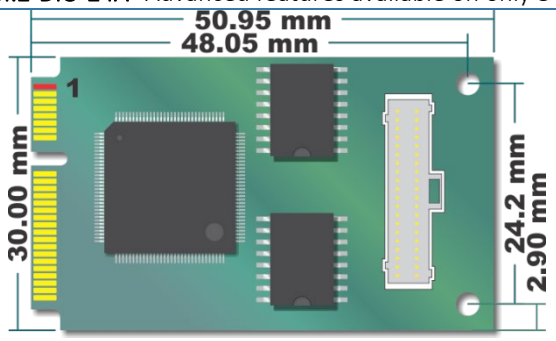
Output Features

- Pulse (high/low), Pulse-train, and PWM generation

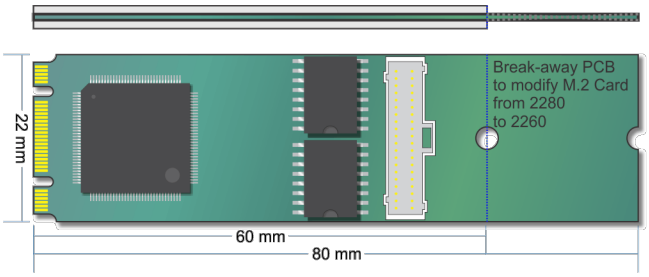
The -24A variants are less flexible than the -24X and only support Digital Integration Features on 8 inputs (Port B only) and 8 outputs (Port A only).

Chapter 3: Hardware

This manual applies to the following models:	
mPCIe-DIO-24X	24 Digital I/O w/Digital Integration Features
mPCIe-DIO-24A	Advanced features available on only 8 bits I/O
M.2-DIO-24X	24 Digital I/O w/Digital Integration Features
M.2-DIO-24A	Advanced features available on only 8 bits I/O



This model is a full-length "F1" mPCIe device (30 × 50.95 mm).



The M.2 model is B & M keyed 2280 with breakaway for use as 2260

All units are RoHS compliant.

INCLUDED IN YOUR PACKAGE

mPCIe-DIO or M.2-DIO card

Available accessories include:	
CAB-mPCIe-DB37M	DB37 cable accessory
ADAP37, STA-37	37-pin Screw Terminal Accessories
mPCIe-HDW-KIT2	Mounting hardware for 2mm
mPCIe-HDW-KIT2.5	Mounting hardware for 2.5mm

Contact the factory for information regarding additional accessories, options, and specials that may be available to best fit your specific application requirements, such as Industrial Temp (-40°C to 85°C).

Chapter 4: Configuration Settings

All configuration of this device is performed through software; there are no jumpers or switches to set.

Chapter 5: PC Interface

This product interfaces with a PC using a PCI Express Mini Card (mPCIe) (or M.2) connection; a small-form-factor, high-performance, rugged peripheral interconnect technology first introduced for use in laptops and other portable computers.

mPCIe's small size and powerful performance, combined with perfect software compatibility with PCI and PCIe peripheral designs, have led to its recent adoption as a go-to standard for embedded Data Acquisition and Control, and many other applications.

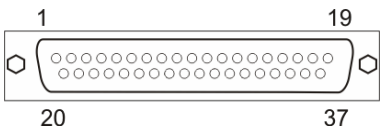
Although mPCIe is a broadly-adopted industry standard, the actual connection to the computer shares a specification with mSATA: both mSATA and mPCIe use the same edge-connector. In fact, well-designed PCs can automatically detect and configure their onboard connectors to work with either mPCIe or mSATA devices – and, according to the standards for mPCIe and mSATA they are *supposed* to do so! However, some PC manufacturers ship computers that *only* support mSATA devices. Please confirm in your PC documentation that your edge-connector is *actually* PCI Express Mini Card compliant before installing this, or any, mPCIe card. Damage might occur if you install an mPCIe device into a computer that only supports mSATA.

mPCIe defines mounting holes for securing the otherwise loose end of the card, so it is impossible for these cards to wiggle or flap themselves loose (which was a recurring problem with the older PCI Mini devices). Eliminating this concern for PCI Express Mini Cards is a major reason this standard has seen rapid adoption by the Data Acquisition and Control industry. Unfortunately, a variety of mounting standoff lengths exist; ACCES offers stand-off kits in both 2mm and 2.5mm sizes. Some computers may provide stand-offs. Please consult your computer manufacturer if it requires a different size.

The mPCIe standard, like its PCI Mini Card predecessor, was designed assuming use primarily in Laptop or Notebook and similar devices, where physical dimension is often the paramount design constraint. In Data Acquisition and Control applications low-weight and vibration tolerance tend to be of more concern.

Chapter 6: I/O Interface

Most customers will use the optional CAB-mPCIe-DB37M's D-Sub Miniature 37-pin Male connector.



CAB-mPCIe-DB37M Male 37-Pin Pinout			
Assignment	Pin		Assignment
Ground	1	20	*Fused +3.3VDC
No Connect	2	21	Ground
DIO 23 (Port CHi bit 7)	3	22	DIO 15 (Port B bit 7)
DIO 22 (Port CHi bit 6)	4	23	DIO 14 (Port B bit 6)
DIO 21 (Port CHi bit 5)	5	24	DIO 13 (Port B bit 5)
DIO 20 (Port CHi bit 4)	6	25	DIO 12 (Port B bit 4)
DIO 19 (Port CLo bit 3)	7	26	DIO 11 (Port B bit 3)
DIO 18 (Port CLo bit 2)	8	27	DIO 10 (Port B bit 2)
DIO 17 (Port CLo bit 1)	9	28	DIO 9 (Port B bit 1)
DIO 16 (Port CLo bit 0)	10	29	DIO 8 (Port B bit 0)
No Connect	11	30	DIO 7 (Port A bit 7)
No Connect	12	31	DIO 6 (Port A bit 6)
No Connect	13	32	DIO 5 (Port A bit 5)
No Connect	14	33	DIO 4 (Port A bit 4)
No Connect	15	34	DIO 3 (Port A bit 3)
*Fused +3.3VDC	16	35	DIO 2 (Port A bit 2)
*Fused +3.3VDC	17	36	DIO 1 (Port A bit 1)
Ground	18	37	DIO 0 (Port A bit 0)
Ground	19		

Notes: Pin 20 is connected to 16 & 17.
***Fused +3.3VDC signals are outputs from the mPCIe bus with standard card version. If TTL Factory Option is ordered, these become User VCCIO inputs which can be 4.5VDC to 5VDC.**

For customers needing deeper integration the on-card connector is a 40-pin latching Molex 501190-4017 connector. The mating connector is the Molex 501189-4010.

40-Pin latching wire-to-board connector			
Assignment	Pin		Assignment
Fused +3.3VDC	40	39	DIO Port C bit 3
Fused +3.3VDC	38	37	DIO Port C bit 2
Fused +3.3VDC	36	35	DIO Port C bit 1
Fused +3.3VDC	34	33	DIO Port C bit 0
Ground	32	31	DIO Port B bit 7
Ground	30	29	DIO Port B bit 6
Ground	28	27	DIO Port B bit 5
Ground	26	25	DIO Port B bit 4
Factory Use Only	24	23	DIO Port B bit 3
Factory Use Only	22	21	DIO Port B bit 2
Factory Use Only	20	19	DIO Port B bit 1
Factory Use Only	18	17	DIO Port B bit 0
Factory Use Only	16	15	DIO Port A bit 7
Factory Use Only	14	13	DIO Port A bit 6
Factory Use Only	12	11	DIO Port A bit 5
Factory Use Only	10	9	DIO Port A bit 4
DIO Port C bit 7	8	7	DIO Port A bit 3
DIO Port C bit 6	6	5	DIO Port A bit 2
DIO Port C bit 5	4	3	DIO Port A bit 1
DIO Port C bit 4	2	1	DIO Port A bit 0

Alternately, custom hardware cables and/or interfaces can be produced to fit your specific application requirement.

Registers (at BAR [1])

Offset (hex)	Register Name	Description
+0	Port A Data	8-bit data register. Bit 0 controls or reports data on digital I/O bit ("DIO") 0 (pin 37). Bit 7 is DIO 7 (pin 30)
+1	Port B Data	8-bit data register. Bit 0 controls or reports data on DIO 8, pin 29. Bit 7 is DIO 15 (pin 22)
+2	Port C Data	8-bit data register. Bit 0 controls or reports data on DIO16, pin 10. Bit 7 is DIO 23 (pin 3). Port C can be configured as two 4-bit groups, each with its own I/O direction.
+3	DIO Control	D7 D6 D5 D4 D3 D2 D1 D0 1 0 0 A CHi 0 B CLo A, B, CHi, CLo direction bits: 1 for input, 0 for output. Set bits A, B, CLo, or CHi to configure the corresponding port for input. Clear the bit for output mode. Examples: D7 D6 D5 D4 D3 D2 D1 D0 Binary Hex Description 1 0 0 0 0 0 0 0 1000 0000 80 All outputs 1 0 0 1 1 0 1 1 1001 1011 9B All inputs
+28	Global IRQ Enable	Write 0xFF to enable IRQs, writes 0x00 to disable. This does not impact which individual IRQ types are enabled in other registers.
+2C	Debounce	D7 D6 D5 D4 D3 D2 D1 D0 x x x x x x x DEB Set DEB to set 1 ms-scale debounce filtering on all filtered bits. Clear bit 0 for µs-scale filtering on filtered bits.
+2D	AutoPulse	D7 D6 D5 D4 D3 D2 D1 D0 x x x x x x x AUTO Set AUTO to enable Automatic Pulse Output. Pulse-train/PWM starts when PulseHIGH is written.
+2E	PWM Divider	8-bit divider of the Pulse/PWM base clock to achieve longer pulses / slower PWM
+30	IRQen / IRQstat	32-bit control register. Set a bit to enable IRQs from the corresponding DIO Event Counter. Clear to disable. Read to detect which DIO bits have IRQs pending. Bits 0 through 23 correspond to DIO 0 through DIO 23. Bits 24 through 31 are unused.
+40	EVENTS	32-bit status register. Read to determine which DIO bits have had (enabled) Events occur since the last read of this register (reading this register clears the bits). Bits 0 through 23 correspond to DIO 0 through DIO 23. Bits 24 through 31 are unused.
+50	GO / DONE	32-bit control / status register. Set a bit to initiate output operations on the corresponding DIO bit. Set multiple GO bits to start multiple outputs simultaneously. Reading will return 1 if the corresponding bit is performing an output process. Bits 0 through 23 correspond to DIO 0 through DIO 23. Bits 24 through 31 are unused.
+98	FPGA Revision	
+A0	Flash ADDR+Dir	These are advanced registers that should be avoided. Misuse can brick your unit. Contact us for details.
+A4	Flash Data	
+A8	Flash Erase	
+FC	RESET	D7 D6 D5 D4 D3 D2 D1 D0 0 0 0 0 0 RESET COUNT QUAD Set QUAD to reset the Quadrature Input counter. Set COUNT to reset all Event Counters. Set RESET to perform a full reset of the FPGA.

There are 240 additional registers associated in groups of 10 with each of the DIO bits. DIO 0's set of 10 registers is located at offset 0x100, DIO 1 at 0x200, etc. i.e. offset = 0x100 * (bit + 1).

<table>
<tr><th colspan="3">Per-DIO Registers (at BAR [1] + DIO# * 100h + 100h) (only DIO 0 shown)</th></tr>
<tr><th>Offset (hex)</th><th>Register Name</th><th>Description</th></tr>
<tr><td>+100</td><td>DEBOUNCE</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>DEBOUNCE</td></tr>
</table>
Set DEBOUNCE to enable the low-pass filter for DIO bit x. DIO8 through 15 do not support filtering. The filter frequency has two settings configured globally (for all DIO) via the DEB bit in the MISC register (+2C)
</td></tr>
<tr><td>+104</td><td>EVENTSen</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>EIRQ</td><td></td><td>EIRQen</td><td></td><td>HIGHp</td><td>LOWp</td><td>RISING</td><td>FALLING</td></tr>
</table>
Set FALLING or RISING to generate an Event when a high-to-low or low-to-high (respectively) transition is detected on this DIO input. Set HIGHp to generate an Event when an input senses a high-going pulse. Set LOWp for low-going pulse Event detection. Set EIRQen to enable the Event Counter to generate IRQs. Read EIRQ to determine if DIO bit x has an Event Counter IRQ pending. Write 1 to EIRQ to clear the pending IRQ (or quickly clear multiple DIO bit's IRQs via the EVENTS register at +40). Note: only one Event can be enabled at a time.
</td></tr>
<tr><td>+108</td><td>EVENTcounter / PULSEcount</td><td>INPUT BITS: 8-bit status register. Read EVENTcounter to check how many enabled events have occurred on this DIO input.
OUTPUT BITS: 8-bit control register. Write PULSEcount to configure how many pulses to generate on this DIO output.</td></tr>
<tr><td>+10C</td><td>EVENTlimit</td><td>8-bit control register. Write EVENTlimit to set how many Events on this DIO input are needed to generate an EVENTS IRQ (if enabled)</td></tr>
<tr><td>+110</td><td>PULSE</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>PulseHigh</td><td>PWM</td><td>Pgo</td></tr>
</table>
Set Pgo to initiate low-going pulse output on this DIO output. Set PulseHigh to generate a high-going pulse. Use PULSEcount to configure how many pulses to generate. Set PWM to generate a Pulse-width modulated ("PWM") waveform (by ignoring PULSEcount).
</td></tr>
<tr><td>+120</td><td>PULSElow / ActivePULSEcounts</td><td>INPUT BITS: 16-bit counter. Read PULSElow for the duration of the most-recently detected low-going pulse. Duration = PULSElow * 8ns.
OUTPUT BITS: 16-bit counter. Write ActivePULSEcounts to configure how long the active-going portion of a pulse, pulse train, or PWM will last. ActivePulseCounts = Desired Duration ÷ 8ns</td></tr>
<tr><td>+124</td><td>PULSEhigh / InactivePULSEcounts</td><td>INPUT BITS: 16-bit counter. Read PULSEhigh for the duration of the most-recently detected low-going pulse. Duration = PULSEhigh * 8ns.
OUTPUT BITS: 16-bit counter. Write InactivePULSEcounts to configure the delay between pulses. InactivePulseCounts = Desired Duration ÷ 8ns</td></tr>
<tr><td>+130</td><td>PWMlow</td><td>16-bit counter. Determine the duty cycle of an input PWM waveform by reading PWMlow and PWMhigh. Duty cycle = PWMhigh ÷ (PWMhigh + PWMlow) *100%. PWMlow differs from PULSElow in that the counter will not measure pulses that occur infrequently.</td></tr>
<tr><td>+134</td><td>PWMhigh</td><td>16-bit counter. Determine the duty cycle of an input PWM waveform by reading PWMlow and PWMhigh. Duty cycle = PWMhigh ÷ (PWMhigh + PWMlow) *100%. PWMhigh differs from PULSEhigh in that the counter will not measure pulses that occur infrequently.</td></tr>
<tr><td>+140</td><td>FREQUENCY</td><td>32-bit counter. Read FREQUENCY to determine the frequency on this DIO input. Frequency = 1 ÷ 8ns * FREQUENCY</td></tr>
</table>

M.2- and mPCIe-DIO-24A note: Unlike the -24**X**, only bits 0-7 support advanced Event detection/IRQs and pulse/PWM/frequency measurement features. Only bits 8-15 support pulse train and PWM generation. Also, only bits 0-7 and 16-23 support debounce. All of these features are supported on all bits in the M.2- and mPCIe-DIO-24X model.

All of these registers can be operated from any operating system using any programming language, using either no driver at all (kernel mode, Linux ioperm(3), DOS, etc.) or using one of the ACCES provided drivers (AIOWDM [for Windows], APCI [for Linux & OSX]), or using any 3rd party APIs such as provided with Real-Time OSes.

In Windows[1], please consult the various samples (C#, Delphi, and more) to explore how to program the device. The Software Reference Manual.pdf provides reference material covering all AIOWDM driver APIs, and tips for simplifying tasks such as Plug-and-Play card detection. Please note that the Software Reference Manual.pdf will include numerous functions that don't apply to this device. A quick reference of the most-applicable functions is provided, below:

[1] *In Linux or OSX please refer to the documentation at* github.com/accesio/apci.

AIOWDM API Quick Reference, DIO w/CoS IRQs	
Function name	Function Purpose
RelInPortL()	Read 32-bits of data
RelOutPortB()	Write 8-bits of data
GetNumCards()	Determine how many cards AIOWDM has detected in the system
COSWaitForIRQ()	Block the thread until the device reports a change-of-state has occurred on a pin of an enabled I/O group (or the wait is aborted).

There are quite a few additional entry points provided by AIOWDM.dll; please consult the Software Reference Manual.pdf, and/or the sample programs, for more information.

Under certain circumstances the following information might prove useful:

PCI Express Mini Card Plug-and-Play Data	
Vendor / Device ID	Card Type
0x494F / 0x2E50	mPCIe-DIO-24A & M.2-DIO-24A
0x494F / 0x2E51	mPCIe-DIO-24X & M.2-DIO-24X

A NOTE ABOUT PERFORMANCE

The PCI Express bus and is capable of very high bandwidth, but the latency per-transaction is roughly the same as all the other busses – it hasn't improved in decades. This means you can expect to usually see a not-less-than 1MHz transaction rate. Typical rates exceed 3MHz [0.3µs].

Unfortunately, modern Operating Systems have introduced a new source of latency, the kernel / userland division. Application code runs in userland, which must transition to the kernel in order to perform any hardware operation. This transition adds quite a lot of latency, which varies between different OSes, motherboards and revisions thereof, etcetera. A Windows XP system can see an additional 7µs per transaction; a modern computer might see 3µs or less. Any transaction from the kernel itself, however, avoids this additional overhead.

Real-time operating systems will enable the highest transaction rates possible, all the way up to the hardware limits.

The latest information can always be found on the product page on the website. Here are some useful links:

Links to useful downloads	
ACCES web site	https://accesio.com
Product web page	accesio.com/mPCIe-DIO-24A, accesio.com/M.2-DIO-24A
This manual	accesio.com/MANUALS/M.2-_mPCIe-DIO-24X.pdf
Install Package	accesio.com/files/packages/mPCIe-DIO-24A Install.exe
Linux / OSX	github.com/accesio/apci

CHAPTER 8: SPECIFICATIONS

PC Interface

PCI Express Mini Card	Type F1 "Full Length" V1.2

Digital Input / Output Interface

Digital Bits		24
Compatibility		8255 Mode 0
Performance		1 µs per 32-bit transaction max ~3.5µs in Windows
Digital Inputs	Logic High Logic Low	2.0V to VCCIO (3.3VDC, 5VDC tolerant) 0V to 0.8V
Digital Outputs (Standard Version)	Logic High Logic Low Power Output	2.0V (min) 24mA source 0.55V (max) 24mA sink +3.3 VDC via 0.5A polyfuse (resetting)
TTL w/user VCCIO Digital Inputs (-TTL Option)	74LVC8T245 Logic High Logic Low	Buffer chip 3.5V to 5V, UVCCIO = 5V 0V to 1.5V, UVCCIO = 5V
TTL w/user VCCIO Digital Outputs (-TTL Option)	1.65V to 5.5V Logic High Logic Low	Supplied by user at DB37M, polyfused 3.8V (min) 32mA UVCCIO = 4.5V 0.55V (max) 32mA UVCCIO = 4.5V

Feature	-24A variant limitation	Description
Debounce Feature	Bits 0-7 and 16-23 only	Enabled per-bit Global filter configuration between ms and µs scale filtering
Pulse Measurement	Bits 0-7 and 16-23 only	Measured using an 8ns, 16-bit clock. Narrowest pulse 8ns, longest 524.28ms
Frequency Measurement	Bits 0-7 and 16-23 only	Measured using an 8ns, 32-bit clock. Fastest frequency 62.5MHz
Event Counter	Bits 0-7 and 16-23 only	Count up to 255 enabled events with 8-bit counter threshold IRQ per bit.
Pulse Generation	Bits 8-15 only	Generate a high or low pulse using 8ns resolution, 16ns to 524.280ms duration

Pulse Train Generation	Bits 8-15 only	Generate between 2 and 255 pulses with 8ns to 524.280ms between them
PWM Generation	Bits 8-15 only	Specify high and low side pulse durations with 8ns resolution.

Environmental

Temperature	Operating	0°C to 70°C (order "-T" for -40° to 85°C)
	Storage	-65° to 150°C
Humidity		5% to 95%, non-condensing
Power required		+3.3VDC @ 330mA (typical)

Physical

Weight		6.2 grams (+ 22.2g for the cable)
Size	Length	50.95mm (2.006")
	Width	30.00mm (1.181")
I/O connector	On-card	Molex 501190-4017 40-pin latching
	mating	Molex 501189-4010
	On cable	Male, D-Sub Miniature, 37-pin
	mating	Female, D-Sub Miniature, 37-pin

Chapter 9: Certifications

CE & FCC

These devices are designed to meet all applicable EM interference and emission standards. However, as they are intended for use installed on motherboards, and inside the chassis of industrial PCs, important care in the selection of PC and chassis is important to achieve compliance for the computer as a whole.

UL & TUV

Neither DC voltages above 3.3V, nor AC voltages of any kind, are consumed or produced during normal operation of this device. This product is therefore exempt from any related safety standards. Use it with confidence!

ROHS / LEAD-FREE STATEMENT

All models are produced in compliance with RoHS and various other lead-free initiatives.

WARNING

A SINGLE STATIC DISCHARGE CAN DAMAGE YOUR CARD AND CAUSE PREMATURE FAILURE! PLEASE FOLLOW ALL REASONABLE PRECAUTIONS TO PREVENT A STATIC DISCHARGE SUCH AS GROUNDING YOURSELF BY TOUCHING ANY GROUNDED SURFACE PRIOR TO TOUCHING THE CARD.

ALWAYS CONNECT AND DISCONNECT YOUR FIELD CABLING WITH THE COMPUTER POWER OFF. ALWAYS TURN COMPUTER POWER OFF BEFORE INSTALLING A CARD. CONNECTING AND DISCONNECTING CABLES, OR INSTALLING CARDS, INTO A SYSTEM WITH THE COMPUTER OR FIELD POWER ON MAY CAUSE DAMAGE TO THE I/O CARD AND WILL VOID ALL WARRANTIES, IMPLIED OR EXPRESSED.

WARRANTY

Prior to shipment, ACCES equipment is thoroughly inspected and tested to applicable specifications. However, should equipment failure occur, ACCES assures its customers that prompt service and support will be available. All equipment originally manufactured by ACCES which is found to be defective will be repaired or replaced subject to the following considerations:

GENERAL

Under this Warranty, liability of ACCES is limited to replacing, repairing or issuing credit (at ACCES discretion) for any products which are proved to be defective during the warranty period. In no case is ACCES liable for consequential or special damage arriving from use or misuse of our product. The customer is responsible for all charges caused by modifications or additions to ACCES equipment not approved in writing by ACCES or, if in ACCES opinion the equipment has been subjected to abnormal use. "Abnormal use" for purposes of this warranty is defined as any use to which the equipment is exposed other than that use specified or intended as evidenced by purchase or sales representation. Other than the above, no other warranty, expressed or implied, shall apply to any and all such equipment furnished or sold by ACCES.

TERMS AND CONDITIONS

If a unit is suspected of failure, contact ACCES' Customer Service department. Be prepared to give the unit model number, serial number, and a description of the failure symptom(s). We may suggest some simple tests to confirm the failure. We will assign a Return Material Authorization (RMA) number which must appear on the outer label of the return package. All units/components should be properly packed for handling and returned with freight prepaid to the ACCES designated Service Center, and will be returned to the customer's/user's site freight prepaid and invoiced.

COVERAGE

FIRST THREE YEARS: Returned unit/part will be repaired and/or replaced at ACCES option with no charge for labor or parts not excluded by warranty. Warranty commences with equipment shipment.

FOLLOWING YEARS: Throughout your equipment's lifetime, ACCES stands ready to provide on-site or in-plant service at reasonable rates similar to those of other manufacturers in the industry.

EQUIPMENT NOT MANUFACTURED BY ACCES

Equipment provided but not manufactured by ACCES is warranted and will be repaired according to the terms and conditions of the respective equipment manufacturer's warranty.

DISCLAIMER

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PCI EXPRESS MINI CARD STANDARD NOTICE AND EXCEPTION

The mPCI-DIO-24Afamily of devices are fully compliant with PCI Express Mini Card v1.2.